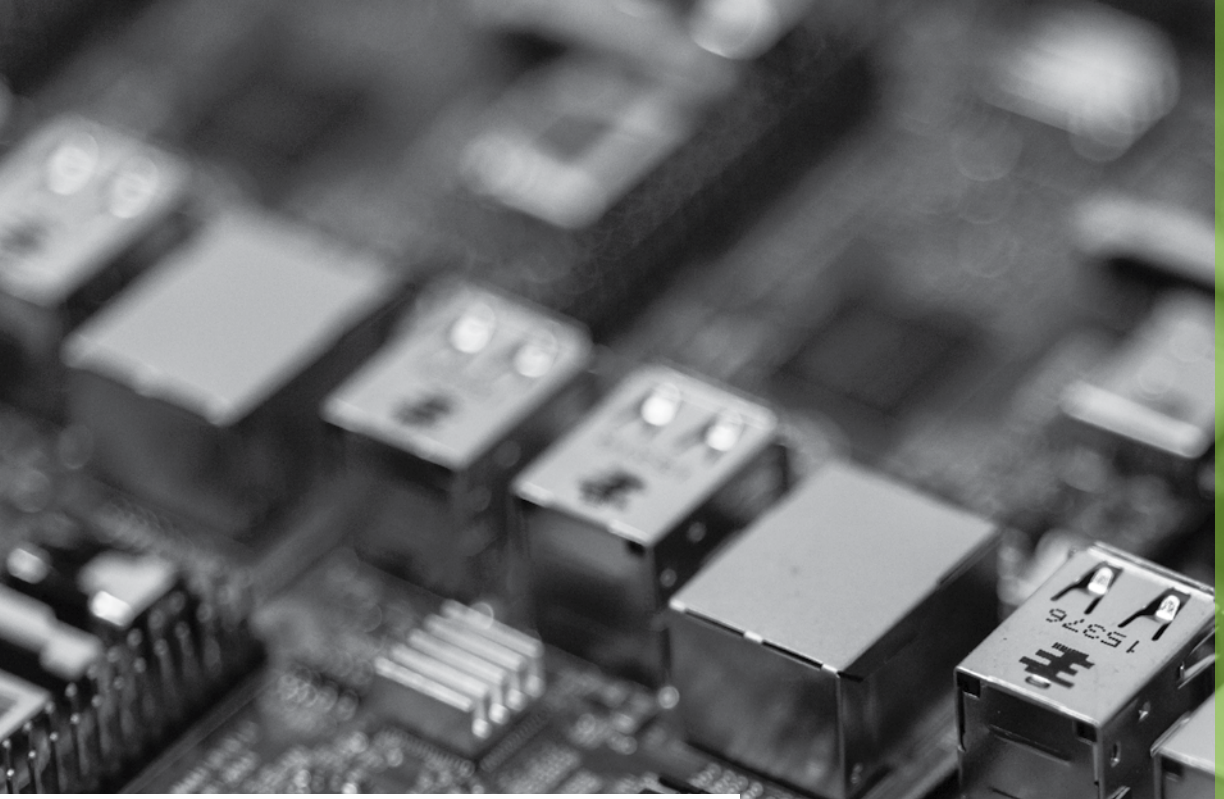

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The workshop is organized within the 34th Edition of the International CAE Conference and Exhibition

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INTERNATIONAL CAE CONFERENCE

WORKSHOP

EXASCALE COMPUTING WORKSHOP: EXPERIENCES AND BEST PRACTICES FOR PORTING APPLICATIONS TO EMERGING HPC ARCHITECTURES AND PLATFORMS

8 - 9 OCTOBER 2018

Vicenza Convention Centre
@Fiera di Vicenza

Via dell’Oreficeria 16
36100 Vicenza | ITALY

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The international race to develop the world's first exascale supercomputer is the next frontier in High Performance Computing (HPC). An exascale computer is one that can complete one quintillion (10^{18}) Floating Point Operations Per Second (FLOPS). This represents a thousand-fold improvement over today's petascale machines which can achieve one quadrillion (10^{15}) flops. One exaflop (Eflops), therefore, equals 1000 petaflops (pflops)[1].

But the creation of an exascale supercomputer requires substantial changes to the current technological models, including in the areas of energy consumption, scalability, network topology, memory, storage, resilience and, consequently, the programming models and systems software – none of which can scale to these performance levels.

Architecturally, existing petascale machines mainly deliver power through multi-core accelerators (Graphics Processing Units (GPUs), Cell Broadband Engine Architecture (Cell) processors, etc.), which have already created challenges for scientific applications. These stumbling blocks will become more evident in future exascale systems as millions of processing units cause parallel application scalability issues (due to sequential application parts having to synchronise their communications) and other bottlenecks.

This means that after the hardware and platforms, applications and systems software for exascale supercomputers need to be redesigned in order to exploit these numbers of computing units more efficiently.

This workshop aims to provide a forum for vanguard users and developers in the HPC arena to share their experiences and achievements around the various European platforms developed by the ExaNeSt, ExaNoDe, Ecoscale and EuroExa projects.

Whether you are designers of new hardware architectures or system components; software or application developers; or users that need to exploit these massive processing capacities, everyone has something valuable to contribute to the discussion in the development of this next frontier of HPC.

All these pioneering experiences provide vital information and perspectives on problems, solutions and challenges to software and hardware developers in the HPC sphere. This feedback is fundamental to assisting the efforts to make these architectures and platforms more widely available to the scientific and technological communities in the next several years, and to secure the economic, technological, scientific and industrial benefits that supercomputing potentially offers to the global challenges facing the world today.

1. See https://kb.iu.edu/d/apeq